

REPLACEMENT SHEET

ATTY DKT. NO.: INFN/WB0037

U.S. SERIAL NO.: 10/720,730

FILED: NOVEMBER 24, 2003

TITLE: DRAM CELL ARRANGEMENT WITH VERTICAL MOS TRANSISTORS, AND METHOD FOR ITS FABRICATION

INVENTOR(S): TILL SCHLÖSSER ET AL.

CONF. NO.: 2757

SHEET 1 OF 3

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FIG 1b

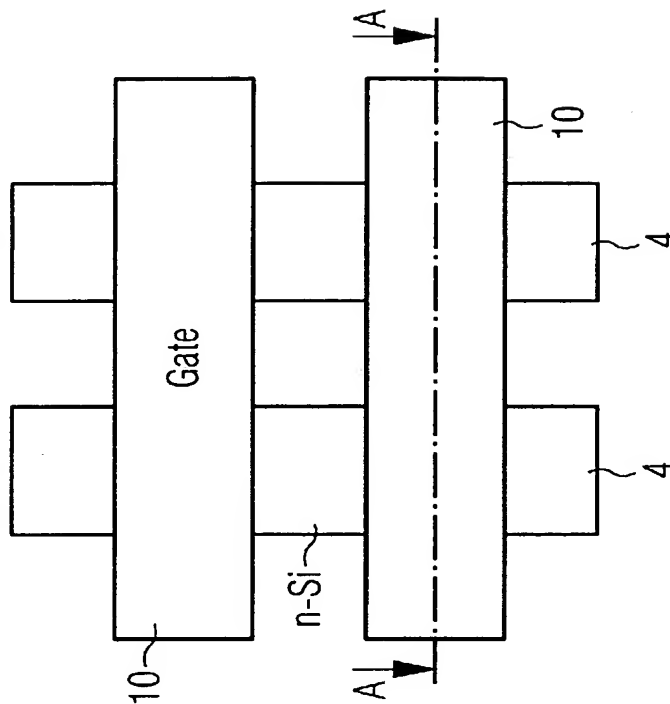
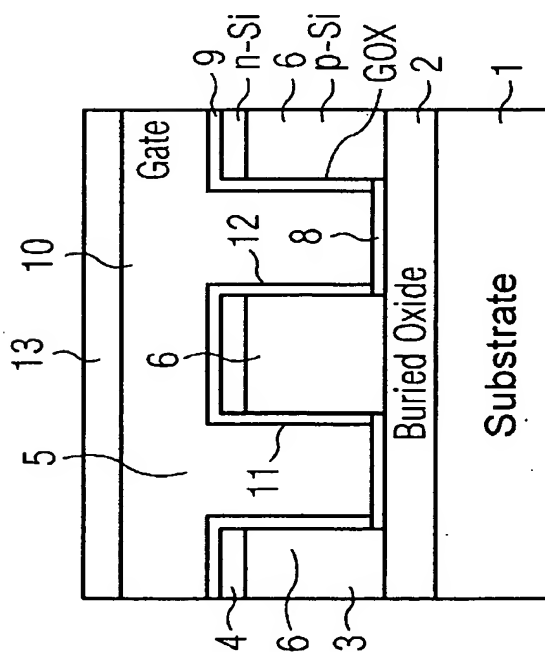


FIG 1a



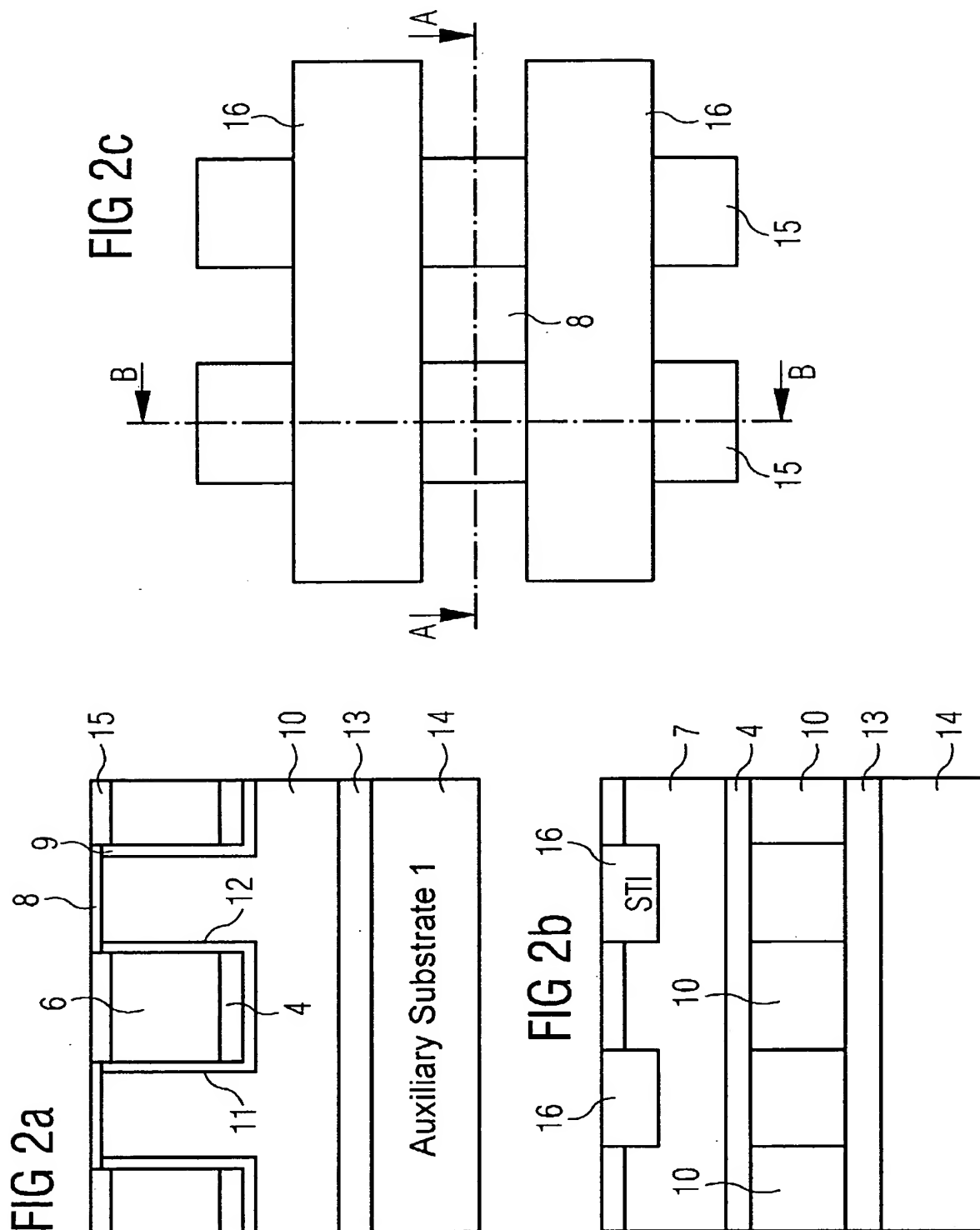
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FIG 4

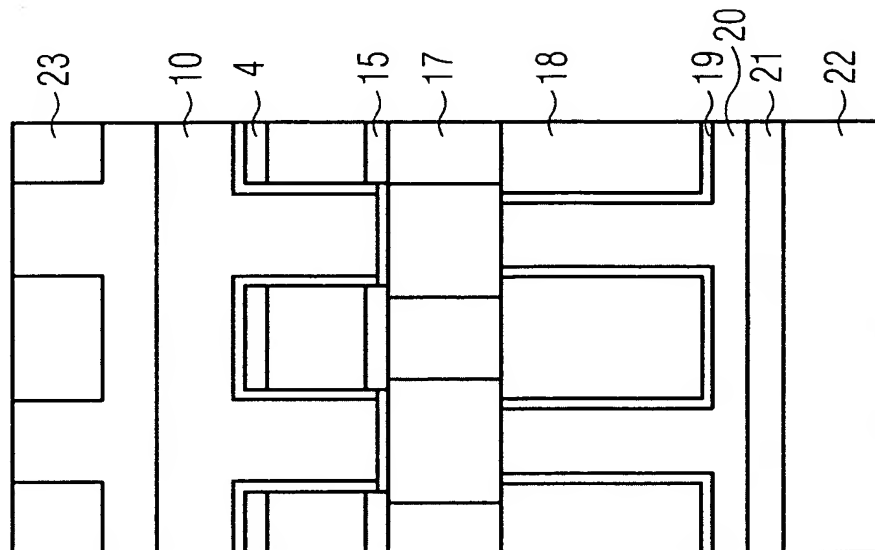


FIG 3

